Application No.: 09/408,429 Atty. Docket No.: EMC2-032PUS
(formerly 07072/086001)

REMARKS/ARGUMENTS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

Claims 6 and 7 have been amended to more clearly and distinctly point out the subject matter applicant regards as his invention. It is respectfully submitted that such calims are now in accordance with 35 USC 112, second paragraph.

Claim 1 has been amended to more clearly point out the subject matter applicant regards as his invention.

Claim 1 stands rejected as being unpatentable over Kadambi et al. (USP 6,335,935) in view of Chin et al., USP 6,356,972)

Claim 1 points out that a ***microprocessor interface*** includes

> (i) a data rebuffering section having a main memory bi-directional data port, a microprocessor bi-directional data port coupled to the microprocessor, and a plurality of additional bi-directional data ports, such data rebuffering section being adapted to selectively couple data from any one of the plurality of additional bi-directional data ports to the microprocessor bi-directional data port selectively in accordance with a control signal; and
>
> (ii) a main memory interface having a main memory interface bi-directional data port coupled to the main memory and an additional main memory interface bi-directional data port connected to the main memory bi-directional data port of the data rebuffering section, such main memory interface providing control signals to the main memory and ***for enabling data transfer between the main memory and the microprocessor through the data rebuffering section***. (emphasis ours)

The Examiner appears to consider the external memory 12 as applicants "main memory" and the CPU 52 as applicant's "microprocessor". Applicant fails to find any description in Kadambi et al. of there being any data transfer between the CPU 52 of Kadambi et al. and the external memory 12 of Kadambi et al.

The Examiner refers to sections of Kadambi et al., provided below; however, Applicant fails to find any description in Kadambi et al. of there being any data transfer

between the CPU 52 of Kadambi et al. and the external memory 12 of Kadambi et al.

Thus, in **Col. 6, lines 45-52:**

> CMIC 40 acts as a gateway between the SOC 10 and the host CPU. The communication can be, for example, along a PCI bus, or other acceptable communications bus. CMIC 40 can provide sequential direct mapped accesses between the host CPU 52 and the SOC 10. CPU 52, through the CMIC 40, will be able to access numerous resources on SOC 10, including MIB counters, programmable registers, status and control registers, configuration registers, ARL tables, port-based VLAN tables, IEEE 802.1q VLAN tables, layer three tables, rules tables, CBP address and data memory, as well as GBP address and data memory. Optionally, the CMIC 40 can include DMA support, DMA chaining and scatter-gather, as well as master and target PCI64.

Applicant fails to find any description of there being any data transfer **between the CPU 52 and the external memory 12.**

In **Col. 10, lines 11-19:**

> The S channel 83 of CPS channel 80 provides a system wide communication path for transmitting system messages, for example, providing the CPU 52 with access to the control structure of the SOC 10. System messages include port status information, including port link status, receive port full, and port statistics, ARL table 22 synchronization, CPU 52 access to GBP 60 and CBP 50 memory buffers and SOC 10 control registers, and memory full notification corresponding to GBP 60 and/or CBP 50.

Applicant fails to find any description of there being any data transfer **between the CPU 52 and the external memory 12.**

In Col. 13, lines 42-50:

> CBM 71, in summary, performs the functions of on-chip FAP (free address pool) management, transfer of cells to CBP 50, packet assembly and notification to the respective egress managers, rerouting of packets to GBP 60 via a global buffer manager, as well as handling packet flow from the GBP 60 to CBP 50. Memory clean up, memory budget management,

channel interface, and cell pointer assignment are also functions of CBM 71.

Applicant fails to find any description of there being any data transfer **between the CPU 52 and the external memory 12.**

In Col. 32, lines 16-26:

If the requested packet is located in CBP 50, the CPID is passed from transaction FIFO 132 to packet FIFO 139. If the requested packet is located in GBP 60, the scheduler initiates a fetch of the packet from GBP 60 to CBP 50; packet FIFO 139 only utilizes valid CPID information, and does not utilize GPID information. The packet FIFO 139 only communicates with the CBP and not the GBP. When the egress seeks to retrieve a packet, the packet can only be retrieved from the CBP; for this reason, if the requested packet is located in the GBP 50, the scheduler fetches the packet so that the egress can properly retrieve the packet from the CBP.

Applicant fails to find any description of there being any data transfer **between the CPU 52 and the external memory 12.**

In Col. 33, lines: 5-16:

FIG. 16 is a block diagram showing some of the elements of CPU interface or CMIC 40. In a preferred embodiment, CMIC 40 provides a 32 bit 66 MHz PCI interface, as well as an I2C interface between SOC 10 and external CPU 52. PCI communication is controlled by PCI core 41, and I2C communication is performed by I2C core 42, through CMIC bus 167. As shown in the figure, many CMIC 40 elements communicate with each other through CMIC bus 167. The PCI interface is typically used for configuration and programming of SOC 10 elements such as rules tables, filter masks, packet handling, etc., as well as moving data to and from the CPU or other PCI uplink. The PCI interface is suitable for high end systems wherein CPU 52 is a powerful CPU and running a sufficient protocol stack as required to support layer two and layer three switching functions. The I2C interface is suitable for low end systems, where CPU 52 is primarily used for initialization. Low end systems would seldom change the

configuration of SOC 10 after the switch is up and running.

Applicant fails to find any description of there being any data transfer **between the CPU 52 and the external memory 12.**

In **Col. 33, lines 44-66:**

> Communication between CMIC 40 and C channel 81/P channel 82 is performed through the use of CP-channel buffers 162 for buffering C and P channel messages, and CP bus interface 163. S channel ARL message buffers 164 and S channel bus interface 165 enable communication with S channel 83. As noted previously, PIO (Programmed Input/Output) registers are used, as illustrated by SCH PIO registers 166 and PIO registers 168, to access the S channel, as well as to program other control, status, address, and data registers. PIO registers 168 communicate with CMIC bus 167 through I2C slave interface 42a and I2C master interface 42b. DMA controller 161 enables chaining, in memory, thereby allowing CPU 52 to transfer multiple packets of data without continuous CPU intervention. Each DMA channel can therefore be programmed to perform a read or write DMA operation. Specific descriptor formats may be selected as appropriate to execute a desired DMA function according to application rules. For receiving cells from PMMU 70 for transfer to memory, if appropriate, CMIC 40 acts as an egress port, and follows egress protocol as discussed previously. For transferring cells to PMMU 70, CMIC 40 acts as an ingress port, and follows ingress protocol as discussed previously. CMIC 40 checks for active ports, COS queue availability and other ingress functions, as well as supporting the HOL blocking mechanism discussed above. CMIC 40 supports single and burst PIO operations; however, burst should be limited to S channel buffers and ARL insert/delete message buffers. Referring once again to I2C slave interface 42a, the CMIC 40 is configured to have an I2C slave address so that an external I2C master can access registers of CMIC 40. CMIC 40 can inversely operate as an I2C master, and therefore, access other I2C slaves. It should be noted that CMIC 40 can also support MIIM through MIIM interface 169. MIIM support is defined by IEEE Standard 802.3u, and will not be further discussed herein. Similarly, other operational aspects of CMIC 40 are outside of the scope of this invention.

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Applicant fails to find any description of there being any data transfer **between the CPU 52 and the external memory 12.**

Further, with regard to Chin et al. (USP 6,356,972) patentee's processor controller 42 and which, as understood, Examiner equates with the applicant's data rebuffering section, does not have the following three types of bi-directional data ports:

(A) a main memory bi-directional data port,

(B) a microprocessor bi-directional data port coupled to the microprocessor, and

(C) a plurality of additional bi-directional data ports (it being noted that the "port" from 50b, 50f is as single bi-directional port),

nor does controller 42 selectively couple data from any one of the plurality of additional bi-directional data ports to the microprocessor bi-directional data port selectively in accordance with a control signal because of the absence of the additional bi-directional data ports.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 05-0889.

Respectfully submitted,

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